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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,706	01/29/2004	Ralf Otremba	IFT979US/I434.102.101	5658

7590 04/04/2005

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,706	OTREMBA, RALF	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01292004, 06172004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4 and 5 recite the limitation "a bent section which, below the underside, forms a connection contact," and "exits from the housing at the underside," respectively. There is no mention of the "underside" in Claim 2. Some clarification is suggested to obtain consistency between claims.

Claim Rejections – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 – 6, 8 – 14, and 16 – 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Bellstein et al. (US 5,719,438).

4. Regarding Claim 1, Bellstein et al. disclose a semiconductor component comprising:

a housing (83,91) (Figure 12),

at least two semiconductor chips (13) (Figure 7) arranged in the housing (Figure 12), wherein each chip has a front side and a rear side and each chip has at least one contact area at the front side (15) (Figure 7), and

at least one contact clip (97) within the housing at the bottom left section having a horizontal plate section (horizontal section of 97), which projects from the housing, and a vertical bend at the left, with a first and second connection area that are opposite one another at the right, and which makes contact with at least two of the chips, its first connection (at T-intersection to right) being applied to the contact area of at least one of the chips and its second connection area (interconnection not shown in Figure) (Col. 15, lines 31 – 36) being applied to the contact area of at least another of the chips to the opposite side of the T-intersection. Although it is not shown that the connection is made to the contact clip, it is inherent to enable contact to an outside lead.

5. Regarding Claims 3 and 11, Bellstein et al. disclose a semiconductor component, wherein the housing (83,91) has a top side and an underside (See Figure 12), the areas of which are greater than the remaining front and rear side areas of the housing, the two chips being accommodated in the housing in such a way that their front and rear sides are at least approximately perpendicular to the top side and underside (See Figure 12).

6. Regarding Claims 4, 5, 12, and 13, Bellstein et al. disclose a semiconductor component wherein the at least one contact clip (87) exits from the housing at a side adjoining the underside and has a bent section, which below the underside, forms a connection contact.

7. Regarding Claims 6 and 14, Bellstein et al. do not explicitly recite that the two chips are power transistors but recite (Col. 7, lines 55 – 56) that "each chip may include any function known in the art for implementation on a semiconductor chip." Hence it is implicit that the

chips could be power transistors, which are known to have source/drain and gate regions with contacts.

8. Regarding Claim 8, Bellstein et al. disclose a semiconductor component, wherein the at least one contact clip makes contact with a contact area of the front sides (Figures 7, 12) of the at least two chips.

9. Regarding Claims 9 and 17, Bellstein et al. disclose a semiconductor component, wherein the at least one contact clip makes contact with a contact area at the front side of at least one of the chips (13, Figure 7) (Figure 12) and at the rear side of the other chip (93).

10. Regarding Claims 10 and 16, Bellstein et al. disclose a semiconductor component comprising:

a housing (83,91) with a top side, an underside, a first side, and a second side,

a first semiconductor chip (left side part of stack 11) (Figure 12) configured within the housing, the first semiconductor chip having a front side, a rear side, and a contact area at the front side (Figure 7),

a second semiconductor chip (adjacent to first chip) configured within the housing, the second semiconductor chip having a front side, a rear side, and a contact area at the front side (Figure 7) and,

at least one contact clip (97) within the housing, which has a plate-type section (horizontal section of 97) which projects from the housing and has a vertical bend at the left with a first and second connection area that are opposite one another at the right and which makes

connection with at least two of the chips, its first connection area (at T-intersection to right) being applied to the contact area of at least one of the chips and its second connection area opposite the first connection area, wherein the first connection area makes contact with the contact area of the first semiconductor chip and the second connection area applied to the contact area of the second semiconductor chip (Col. 15, lines 31 – 36). Although it is not shown that the second connection is made to the contact clip, it is inherent to provide contact to an outside lead.

11. Regarding Claim 18, Bellstein et al. disclose that the contact area of the first semiconductor is at the rear side and the contact area of the second is at the rear, wherein the rear is facing to the right (Figure 12).

Claim Rejections – 35 U.S.C. 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 2, 7, and 15 are rejected under 35 U.S.C.103(a) as being unpatentable over Bellstein et al., as applied to Claims 1, 3 – 6, 8 – 14, and 16 – 18 and further in view of Huang et al. (US 6,784,488 B2).

14. Regarding Claims 2, 7, and 15, Bellstein et al. do not disclose the presence of a contact area at the front and rear sides wherein the gate and source areas are formed at the front and the drain contact formed at the rear. Bellstein et al. do disclose (Col. 7, lines 55 – 56) that the chips may be of any description found in the art, as discussed for Claim 6, such as power transistor. However, power transistors are routinely fabricated with the gate and source contacts at the front of the device and the drain contacts at the rear. For example, Huang et al. disclose a power transistor wherein the gate (11) (Figure 8) and source contact (23) is at the front surface and the drain contact (24) is at the rear surface. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power transistor of Huang et al. with Bellstein et al. to produce a vertically stacked array of power MOSFETs with improved reliability.

Conclusions

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
February 22, 2005

EDDIE LEE
SPE TC2800